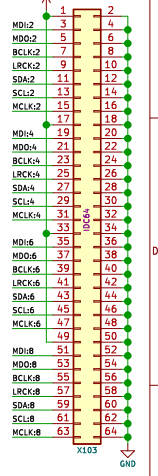
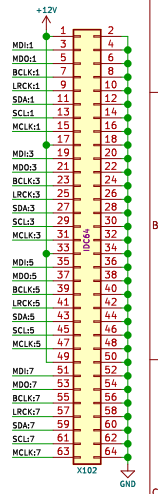
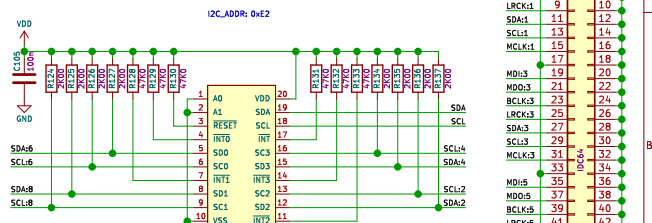
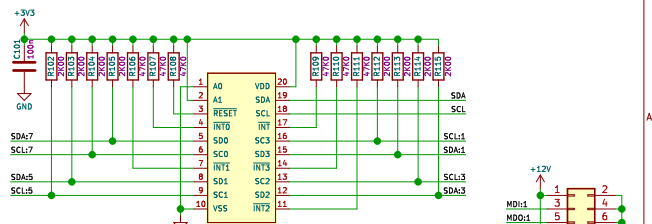
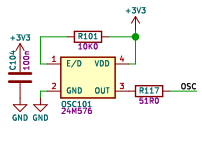
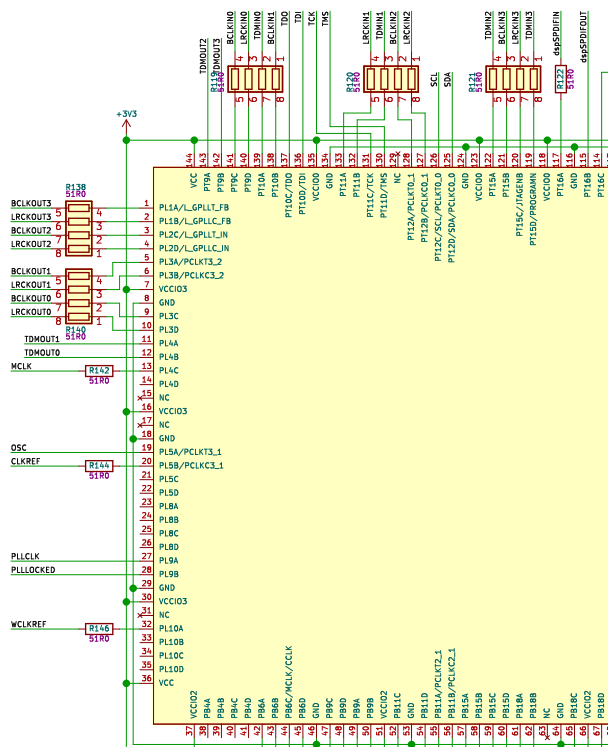


DSP

TDMIN3	DTMIN3	TDMOUT3	TDMOUT3
LRCKIN3	DLRCKIN3	BCLKOUT3	BCLKOUT3
BCLKIN3	DBCLKIN3	LRCKOUT3	LRCKOUT3
TDMIN2	DTMIN2	TDMOUT2	TDMOUT2
LRCKIN2	DLRCKIN2	BCLKOUT2	BCLKOUT2
BCLKIN2	DBCLKIN2	LRCKOUT2	LRCKOUT2
TDMIN1	DTMIN1	TDMOUT1	TDMOUT1
LRCKIN1	DLRCKIN1	BCLKOUT1	BCLKOUT1
BCLKIN1	DBCLKIN1	LRCKOUT1	LRCKOUT1
TDMIN0	DTMIN0	TDMOUT0	TDMOUT0
LRCKIN0	DLRCKIN0	BCLKOUT0	BCLKOUT0
BCLKIN0	DBCLKIN0	LRCKOUT0	LRCKOUT0
SPDFIN	SPDFIN	SPDFOUT	SPDFOUT
MLCK	DMCLK	USRST	USRST
SCL	DSCL		
SDA	DSDA		
RST			

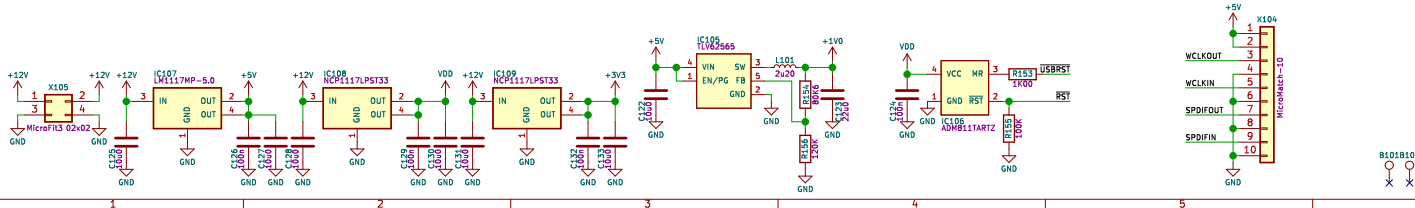
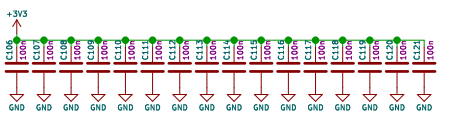
File: dsp.sch



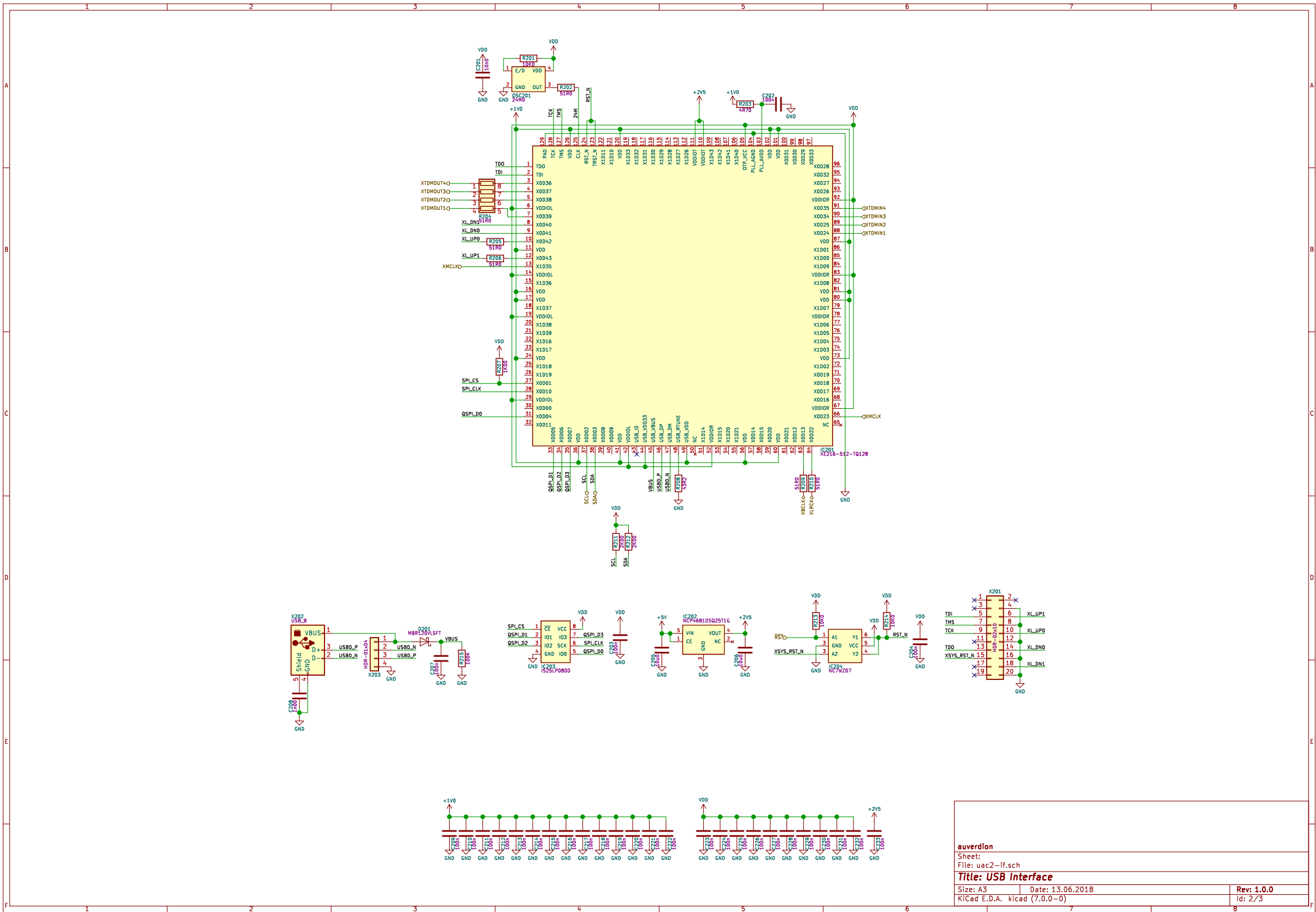
UAC2 Interface

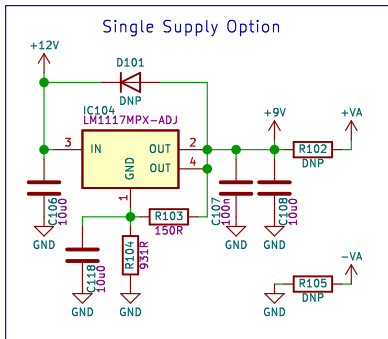
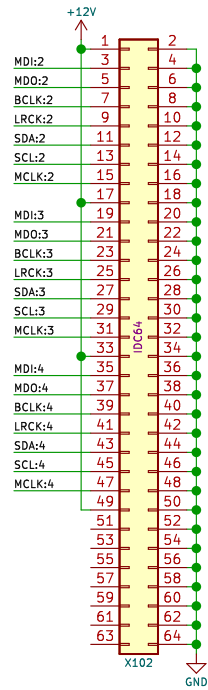
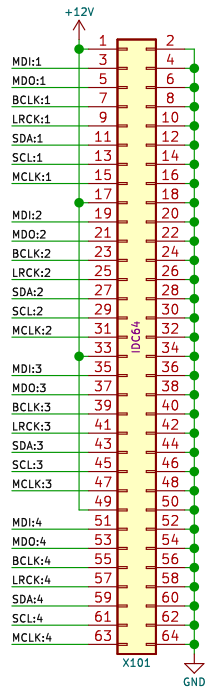
XTDMIN1	XTDMIN1	XTDMOUT1	XTDMOUT1
XTDMIN2	XTDMIN2	XTDMOUT2	XTDMOUT2
XTDMIN3	XTDMIN3	XTDMOUT3	XTDMOUT3
XTDMIN4	XTDMIN4	XTDMOUT4	XTDMOUT4
XMKLK	DXMKLK	SCL	SCL
XRCK	DXRCK	SDA	SDA
RST	DRST		

File: uac2-rsch

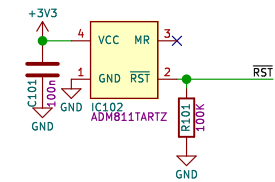
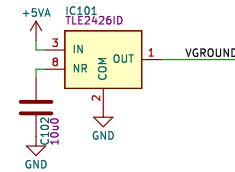
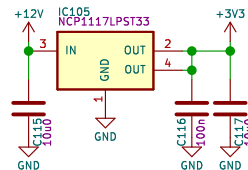
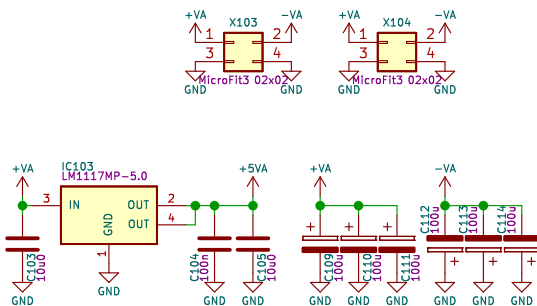


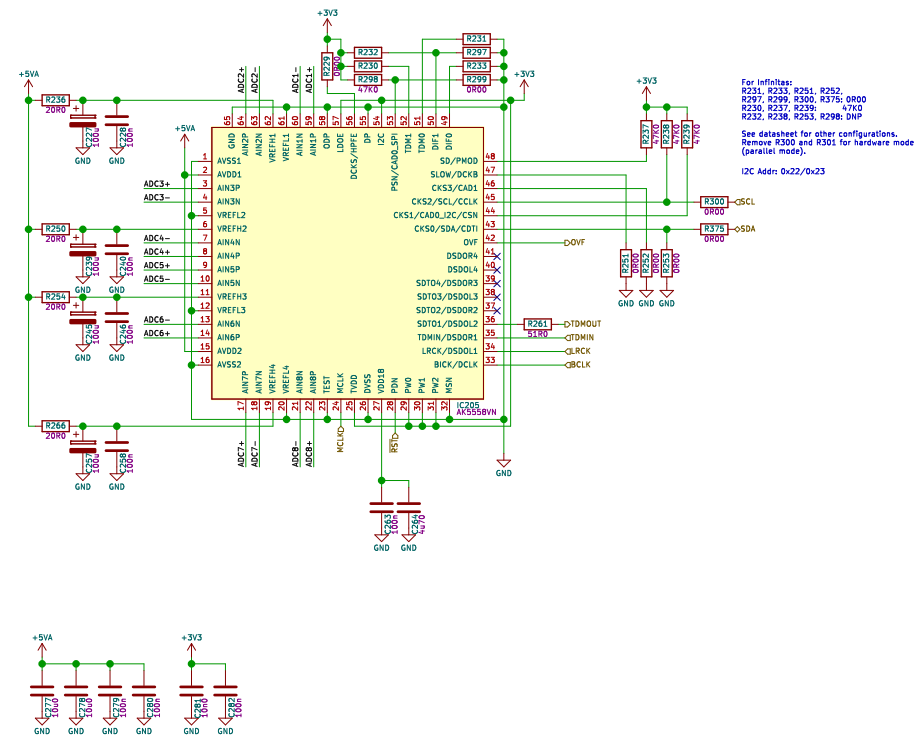
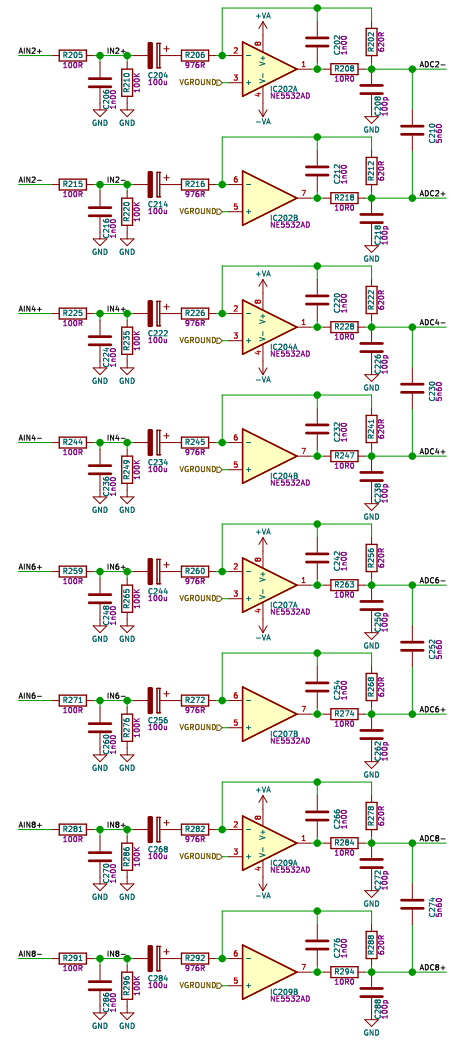
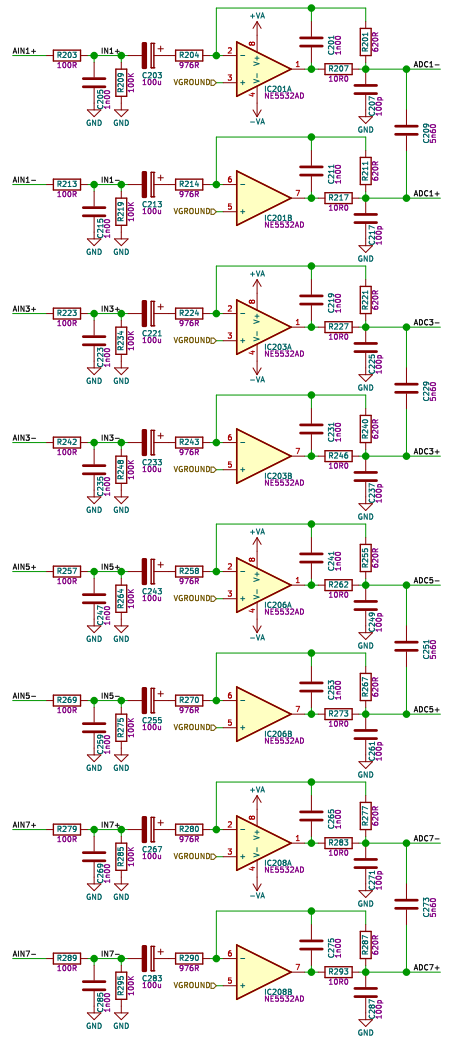
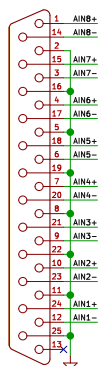
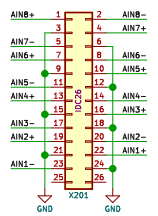
auverdon
 Sheet:
 File: infinitas.sch
Title: FPGA
 Size: A3 Date: 13.06.2018
 KiCad E.D.A. kicad (7.0.0-0) Rev: 1.0.0
 Id: 1/3



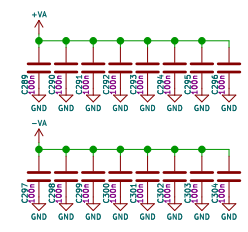


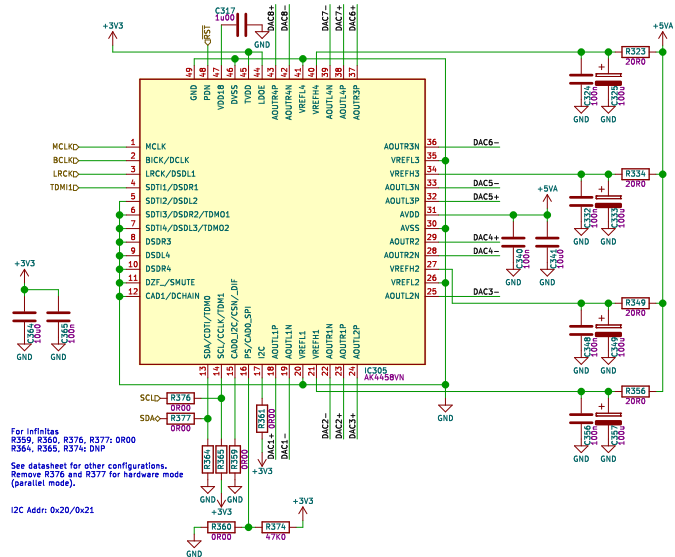
Populate R102 and R105 with 0R00 for single supply





For Infallter:
 R231, R233, R251, R252, R297, R299, R300, R375: 0600
 R230, R231, R239: 4700
 R232, R236, R255, R298: DNP
 See datasheet for other configurations.
 Remove R300 and R301 for hardware mode (parallel mode).
 I2C Addr: 0x22/0x23





For Infinitas
 R359, R360, R376, R377: 0R00
 R364, R365, R374: DNP

See datasheet for other configurations.
 Remove R376 and R377 for hardware mode
 (parallel mode).

I2C Addr: 0x20/0x21

